IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Kamashita
Application Number: 09/925,905
Filing Date: August 9, 2001
Title: Solid Picture Element Manufacturing Method

Date of Amendment: May 27, 2003

Examiner: Brock II, Paul E.
Art Unit: 2815

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PETITION FROM FINAL RESTICTION REQUIREMENT

Commissioner for Patents
PO Box 1450
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Applicant hereby petitions for reconsideration of the final restriction requirement set forth in the Patent and Trademark Office action dated December 26, 2002.

In a Patent and Trademark Office action dated June 25, 2002, a restriction requirement was imposed under 35 U.S.C. 121 to restrict the application to one of the following groups of claims as defined below by the Examiner:

a. Species I depicted in figures 5a- 5c;

b. Species II depicted in figures 6a- 6c;

c. Species III depicted in figures 7a- 7c; and

d. Species IV depicted in figures 8a- 8c.

Applicant elected with traverse the claims of Species I, identifying claims 18-24 and 40-46 are readable on the elected species. Applicant traversed and requested reconsideration of the restriction requirement because at least claim 18 is generic to the claims of Species I as well as to the claims of Species II, III, and IV.

Applicant further noted that claims 47-49 are readable on Species II, claims 50-53 are readable on Species III, and claims 54 and 55 are readable on Species IV. At least claim 18 is generic to elected claims 40-46, as well as claims 47-55 of Species II-IV.

In the office action dated December 26, 2002, the Examiner states that

> The traversal is on the ground(s) that claim 18 is generic to all species I - IV. This is not found persuasive because a quick review of figures 5a-5c clearly shows that the claim limitation in claim 18 of "locating a transfer gate on the first surface of the semiconductor substrate such that the transfer gate overlaps a portion of the charge accumulation region," is not depicted in figures 5a-5c, elected species I. Therefore, claims 18 - 24 have been treated as part of the non-elected species.

Applicant submits that the feature "locating a transfer gate on the first surface of the semiconductor substrate such that the transfer gate overlaps a portion of the charge accumulation region" is included in Fig. 5c (elected Species I), as well as in the figures corresponding to Species II-IV. Applicant submits that claim 18 is therefore generic to all Species and the restriction requirement should be REVERSED.

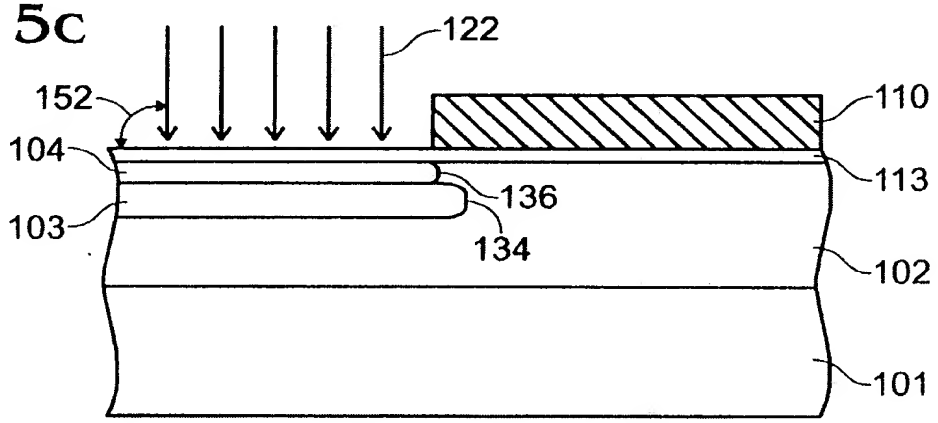
Claim 18 recites:

> A method of transferring a charge from a charge accumulation layer to a transistor of a solid picture element so as to substantially eliminate residual images, comprising the steps:
>
> locating a charge accumulation region of a first conductive type within a semiconductor substrate having a first surface such that no portion of the charge accumulation region contacts the first surface of the semiconductor substrate;
>
> locating a depletion prevention region within the semiconductor substrate between the charge accumulation region and the first surface;
>
> locating a transfer gate on the first surface of the semiconductor substrate such that the transfer gate overlaps a portion of the charge accumulation region; and
>
> locating a transistor within the semiconductor substrate, the transistor being in communication with the transfer gate for receiving a charge from the charge accumulation region and amplifying the charge.

Claim 18 is generic to the claims of Species I, II, III, and IV for the following reasons.

Fig. 5c (Species I) illustrates the result of processing steps including those illustrated by Figs. 5a and 5b.

Fig. 5c



As described in the application beginning at page 14, line 9, Fig. 5c shows formation of a P-type charge accumulation layer 103 and an N-type depletion prevention layer 104. A transfer gate 110 is shown. The distance that the P-type charge accumulation layer 103 projects from the N-type depletion prevention layer 104 is controlled to a desired value.

The Examiner states that Fig. 5c does not show "locating a transfer gate [110] on the first surface of the semiconductor substrate such that the transfer gate [110] overlaps a portion of the charge accumulation region [103]." Applicant submits that Fig. 5c clearly shows the contrary, that the end 134 of charge accumulation region 103 is overlapped by transfer gate 110.

In addition, applicant submits that Fig. 5c shows all features of claim 18:

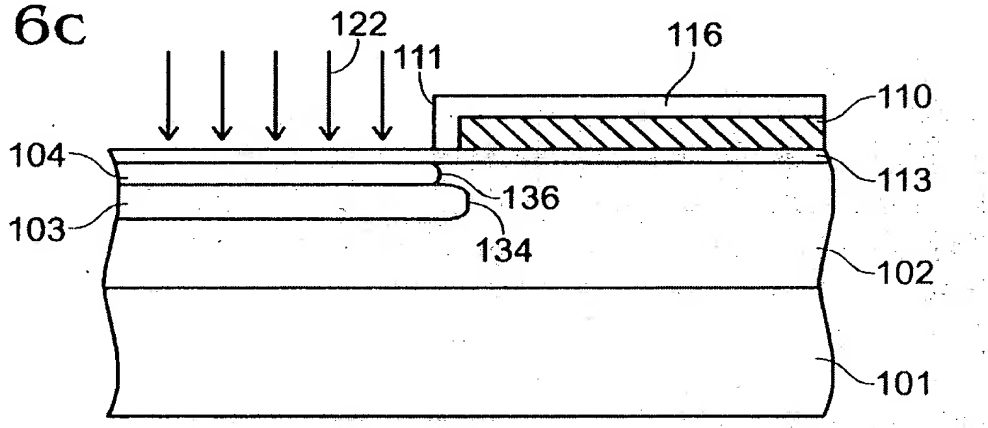
> locating a charge accumulation region [103] of a first conductive type within a semiconductor substrate having a first surface [surface bearing 113] such that no portion of the charge accumulation region [103] contacts the first surface of the semiconductor substrate;
>
> locating a depletion prevention region [104] within the semiconductor substrate between the charge accumulation region [103] and the first surface;
>
> locating a transfer gate [110] on the first surface of the semiconductor substrate such that the transfer gate [110] overlaps a portion of the charge accumulation region [103]; and

locating a transistor within the semiconductor substrate, the transistor being in communication with the transfer gate [110] for receiving a charge from the charge accumulation region and amplifying the charge [analogous to claim 40].

Elected claims 40-46 of Species I further specify other features, including the angle of incidence of ions 122. Applicant submits that claim 18 is generic as to elected Species I of Fig. 5c, particularly with regard to the transfer gate 110 overlapping the charge accumulation region 103. Applicant submits, therefore, that the restriction requirement between elected claims 40-46 and claims 18-24 is improper and should be REVERSED.

Fig. 6c (Species II) illustrates the result of processing steps including those illustrated by Figs. 6a and 6b.

Fig. 6c



As described in the application beginning at page 15, line 16, Fig. 6c shows formation of a P-type charge accumulation layer 103 and an N-type depletion prevention layer 104. A transfer gate 110 with an oxide film 116 is shown. The distance that the P-type charge accumulation layer 103 projects from the N-type depletion prevention layer 104 is controlled to a desired value.

By the final restriction requirement the Examiner implies that Fig. 6c does not show "locating a transfer gate [110] on the first surface of the semiconductor substrate such that the transfer gate [110] overlaps a portion of the charge accumulation region [103]." Applicant submits that Fig. 6c clearly shows the contrary, that the end 134 of charge accumulation region

103 is overlapped by transfer gate 110 and its oxide film 116. As stated at page 15, line 28, oxide film 116 increases the volume of transfer gate 110.

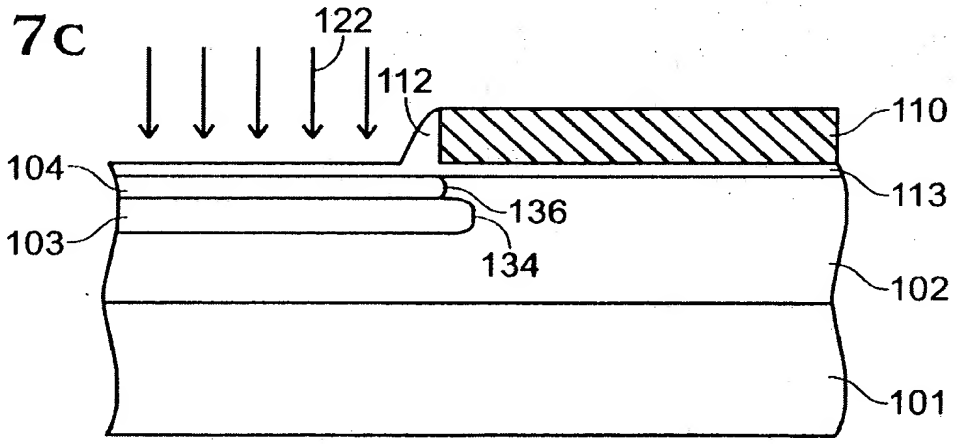
Applicant submits that Fig. 6c shows all features of claim 18:

> locating a charge accumulation region [103] of a first conductive type within a semiconductor substrate having a first surface [surface bearing 113] such that no portion of the charge accumulation region [103] contacts the first surface of the semiconductor substrate;
>
> locating a depletion prevention region [104] within the semiconductor substrate between the charge accumulation region [103] and the first surface;
>
> locating a transfer gate [110] on the first surface of the semiconductor substrate such that the transfer gate [110] overlaps a portion of the charge accumulation region [103]; and
>
> locating a transistor within the semiconductor substrate, the transistor being in communication with the transfer gate [110] for receiving a charge from the charge accumulation region and amplifying the charge [analogous to claim 47].

Claims 47-49 of Species II further specify other features, including formation of an oxide film 116. Applicant submits that claim 18 is generic as to elected Species II of Fig. 6c, particularly with regard to the transfer gate 110 overlapping the charge accumulation region 103. Applicant submits, therefore, that the restriction requirement between elected claims 47-49 and claims 18-24 is improper and should be REVERSED.

Fig. 7c (Species III) illustrates the result of processing steps including those illustrated by Figs. 7a and 7b.

Fig. 7c



As described in the application beginning at page 16, line 18, Fig. 7c shows formation of a P-type charge accumulation layer 103 and an N-type depletion prevention layer 104. A transfer gate 110 with a side wall insulating film 112 is shown. The distance that the P-type charge accumulation layer 103 projects from the N-type depletion prevention layer 104 is controlled to a desired value.

By the final restriction requirement the Examiner implies that Fig. 7c does not show "locating a transfer gate [110] on the first surface of the semiconductor substrate such that the transfer gate [110] overlaps a portion of the charge accumulation region [103]." Applicant submits that Fig. 7c clearly shows the contrary, that the end 134 of charge accumulation region 103 is overlapped by transfer gate 110.

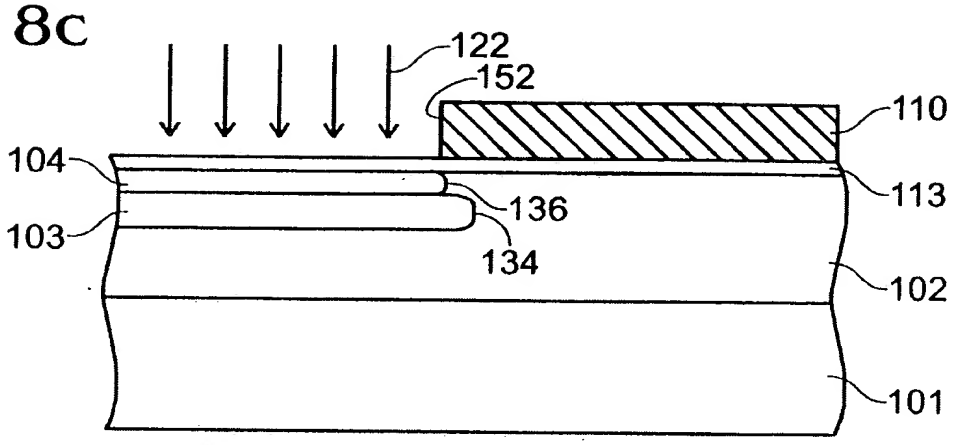
Applicant submits that Fig. 7c shows all features of claim 18:

> locating a charge accumulation region [103] of a first conductive type within a semiconductor substrate having a first surface [surface bearing 113] such that no portion of the charge accumulation region [103] contacts the first surface of the semiconductor substrate;
>
> locating a depletion prevention region [104] within the semiconductor substrate between the charge accumulation region [103] and the first surface;
>
> locating a transfer gate [110] on the first surface of the semiconductor substrate such that the transfer gate [110] overlaps a portion of the charge accumulation region [103]; and
>
> locating a transistor within the semiconductor substrate, the transistor being in communication with the transfer gate [110] for receiving a charge from the charge accumulation region and amplifying the charge [analogous to claim 47].

Claims 50-53 of Species III further specify other features, including formation of an insulating film 112. Applicant submits that claim 18 is generic as to elected Species III of Fig. 7c, particularly with regard to the transfer gate 110 overlapping the charge accumulation region 103. Applicant submits, therefore, that the restriction requirement between elected claims 50-53 and claims 18-24 is improper and should be REVERSED.

Fig. 8c (Species IV) illustrates the result of processing steps including those illustrated by Figs. 8a and 8b.

Fig. 8c



As described in the application beginning at page 17, line 17, Fig. 8c shows formation of a P-type charge accumulation layer 103 and an N-type depletion prevention layer 104. A transfer gate 110 with an end wall 152 is shown. The distance that the P-type charge accumulation layer 103 projects from the N-type depletion prevention layer 104 is controlled to a desired value.

By the final restriction requirement the Examiner implies that Fig. 8c does not show "locating a transfer gate [110] on the first surface of the semiconductor substrate such that the transfer gate [110] overlaps a portion of the charge accumulation region [103]." Applicant submits that Fig. 8c clearly shows the contrary, that the end 134 of charge accumulation region 103 is overlapped by transfer gate 110.

Applicant submits that Fig. 8c shows all features of claim 18:

> locating a charge accumulation region [103] of a first conductive type within a semiconductor substrate having a first surface [surface bearing 113] such that no portion of the charge accumulation region [103] contacts the first surface of the semiconductor substrate;
>
> locating a depletion prevention region [104] within the semiconductor substrate between the charge accumulation region [103] and the first surface;
>
> locating a transfer gate [110] on the first surface of the semiconductor substrate such that the transfer gate [110] overlaps a portion of the charge accumulation region [103]; and
>
> locating a transistor within the semiconductor substrate, the transistor being in communication with the transfer gate [110] for

receiving a charge from the charge accumulation region and amplifying the charge [analogous to claim 54].

Claims 54 and 55 of Species IV further specify other features, including formation of an end wall 152. Applicant submits that claim 18 is generic as to elected Species IV of Fig. 8c, particularly with regard to the transfer gate 110 overlapping the charge accumulation region 103. Applicant submits, therefore, that the restriction requirement between elected claims 53 and 55 and claims 18-24 is improper and should be REVERSED.

Applicant therefore requests that claim 18 be held generic as to the claims of Species I-IV and that the restriction requirement as to the claims of Species I-IV be REVERSED.

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Respectfully Submitted,

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